AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of forming a local interconnect on a semiconductor integrated circuit, the method comprising:

forming a gate stack on a substrate, the gate stack having at least one conductive layer and a source layer positioned on top of the at least one conductive layer, the source layer providing a source of transforming atoms;

exhuming a first layer of the gate stack so as to expose a portion of the source layer;

depositing a refractory material on the integrated circuit so that the refractory material contacts the exposed portion of the source layer of the gate stack and so that the refractory material is positioned on another device of the integrated circuit; and

transforming the refractory material at the exposed portion of the source layer into a low resistance contact between the refractory material and the source layer such that electrical contact between the refractory metal and the at least one conductive level occurs through the source level and wherein the source layer provides transforming atoms to the portion of the refractory material positioned adjacent the exposed portion of the source layer.

2. (Original) The method of Claim 1, further comprising removing excess refractory material, wherein the source layer provides the transforming atoms to the refractory material during transformation of the refractory material to reduce undercutting of the low resistance contact at the exposed surface of the source layer.

3. (Original) The method of Claim 1, wherein the transforming of the refractory material comprises transforming the refractory material adjacent the source layer into a silicide contact and wherein the transforming atoms of the source layer comprise silicon atoms to transform the refractory material adjacent the source layer into the low resistance contact.

4. (Original) The method of Claim 3, wherein forming a gate stack comprises:

depositing a plurality of blanket layers over a semiconductor substrate; and

removing material from the plurality of blanket layers so as to define the gate stack.

5. (Original) The method of Claim 4, wherein depositing a plurality of blanket layers over a semiconductor substrate comprises depositing a blanket gate oxide layer over the substrate.

6. (Original) The method of Claim 5, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing an outwardly conductive blanket layer over the blanket gate oxide layer.

7. (Original) The method of Claim 6, wherein depositing an outwardly conductive blanket layer comprises depositing a first blanket polysilicon layer.

8. (Original) The method of Claim 7, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing a laterally conductive blanket layer over the outwardly conductive blanket layer.

9. (Original) The method of Claim 8, wherein depositing a laterally conductive blanket layer comprises depositing a blanket layer of tungsten silicide.

10. (Original) The method of Claim 9, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing a blanket source layer over the blanket conducting layer.

11. (Original) The method of Claim 10, wherein depositing a blanket source layer over the blanket conducting layer comprises depositing a second blanket polysilicon layer.

12. (Original) The method of Claim 11, wherein depositing a second blanket polysilicon layer comprises depositing a second blanket polysilicon layer having a thickness between 100 Angstroms and 1000 Angstroms.

13. (Original) The method of Claim 4, wherein removing material from the plurality of blanket layers comprises:

forming a mask layer over the plurality of blanket layers that defines the gate stack; and

etching the exposed material from the plurality of blanket layers.

14. (Original) The method of Claim 1, wherein exhuming a first layer of the gate stack comprises removing a portion of a cap insulating layer.

15. (Original) The method of Claim 2, wherein depositing refractory material on the integrated circuit comprises depositing a blanket layer of titanium.

16. (Original) The method of Claim 15, wherein depositing a blanket layer of titanium comprises depositing a blanket layer of titanium having a thickness between 100 Angstroms and 500 Angstroms.

17. (Original) The method of Claim 2, wherein transforming the refractory material comprises annealing the refractory material.

18. (Original) The method of Claim 17, wherein annealing the refractory material comprises exposing the refractory material to a rapid thermal processing environment having an N2/NH3 ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60 seconds.

19. (Original) The method of Claim 2, wherein removing the excess refractory material comprises:

forming a mask layer above the refractory material that defines the extent of the local interconnect before annealing the refractory material; and

etching the exposed refractory material after annealing the refractory material.

20. (Currently Amended) A method of forming a local interconnect on a semiconductor integrated circuit, the method comprising:

forming a gate stack having at least one conductive layer and a source layer of polysilicon positioned on top of the at least one conductive layer, the source layer of polysilicon providing a source of silicon atoms;

exhuming a first layer of the gate stack so as to expose a portion of the source layer;

depositing a refractory material on the integrated circuit so that a portion of the refractory material contacts the exposed portion of the source layer of the gate stack and so that the refractory material is positioned on another device of the integrated circuit;

transforming the portion of the refractory material adjacent the exposed portion of the source layer into a conductive silicide contact such that electrical contact between the refractory metal and the at least one conductive layer occurs through the source layer wherein the source layer provides silicon atoms to the portion of the refractory material positioned adjacent the exposed portion of the source layer; and

removing the excess refractory material such that the conductive silicide contact is substantially preserved wherein the source layer provides sufficient silicon atoms to the refractory material during transformation of the refractory material to reduce undercutting of the conductive silicide contact at the exposed surface of the source layer.

21. (Original) The method of Claim 20, wherein forming a gate stack having at least one conductive layer and a source layer of polysilicon positioned on top of the at least one conductive layer comprises forming a gate stack with a refractory silicide layer immediately underneath a source layer of polysilicon.

22. (Original) The method of Claim 21, wherein forming a gate stack with a refractory silicide layer immediately underneath a source layer of polysilicon comprises forming a gate stack with a tungsten silicide layer immediately underneath a source layer of polysilicon.

23. (Original) The method of Claim 20, wherein depositing refractory material on the integrated circuit comprises depositing a blanket layer of refractory material comprised of titanium.

24. (Original) The method of Claim 23, wherein transforming the refractory material comprises annealing the refractory material.

25. (Currently Amended) The method of Claim 24, wherein removing the excess refractory material comprises.

forming a mask layer above the refractory material that defines the extent of the local interconnect before annealing the refractory material; and

etching the exposed refractory material after annealing the refractory material[[;]].